

e2v

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EV12DS130

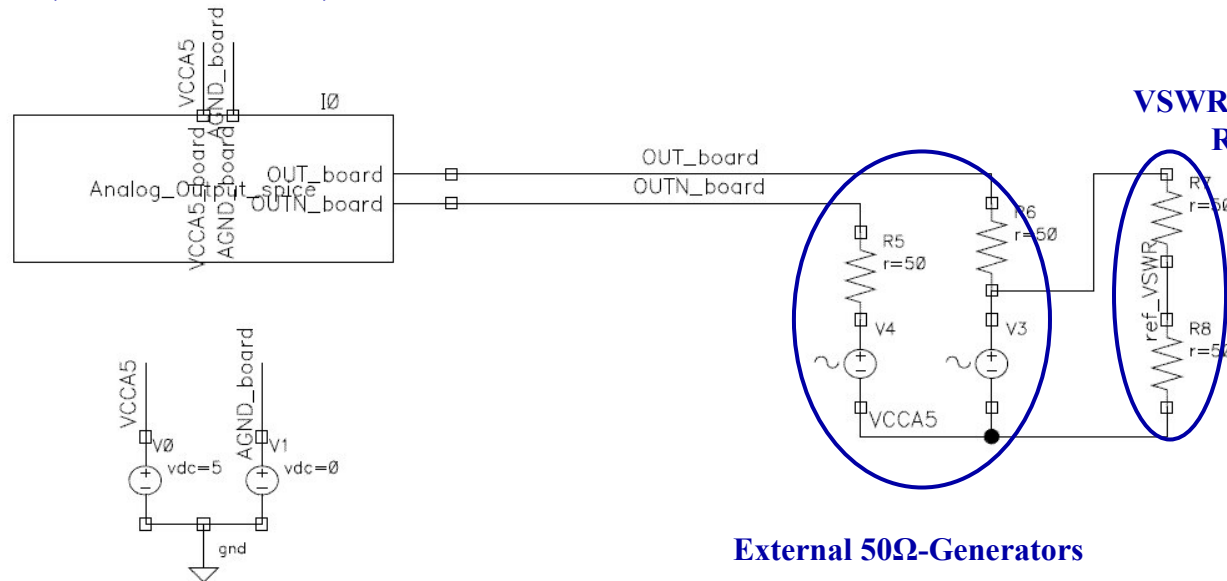
Spice Models

Analog Output Buffer (VSWR)

Top Level Simulation Schematic (simplified model) (VSWR)

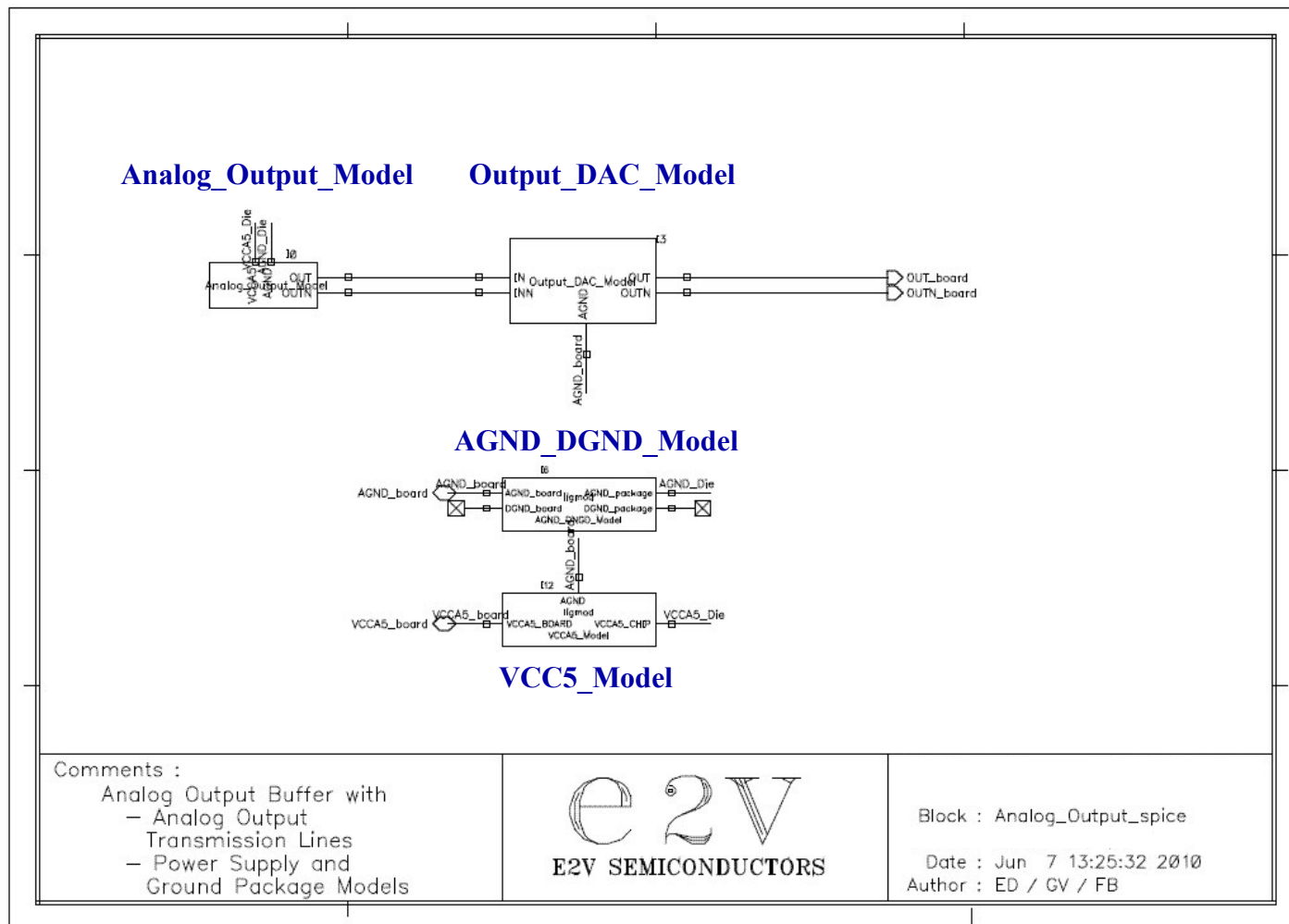
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Analog_Output_spice
(described hereafter)



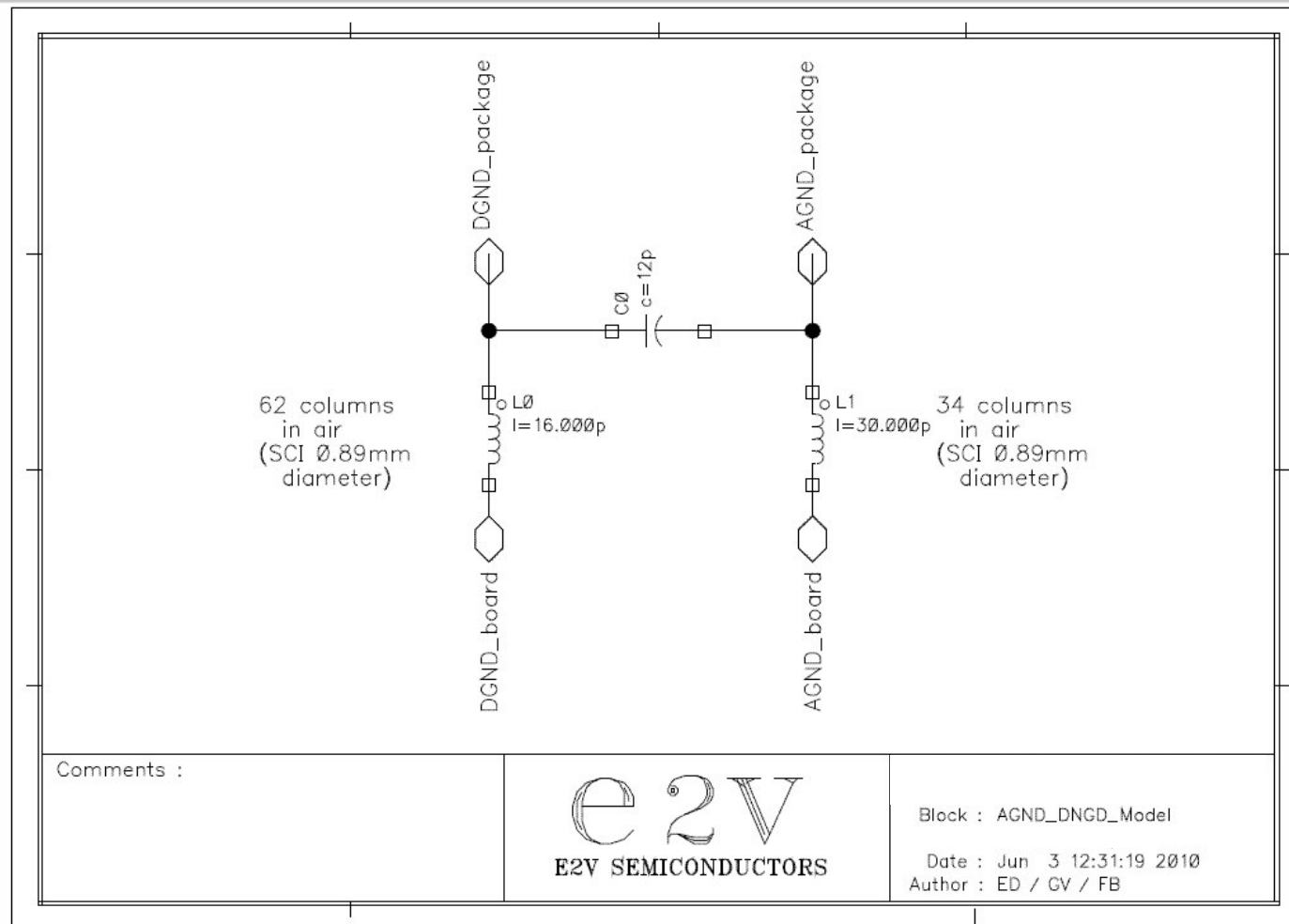
TOP Analog Output Schematic

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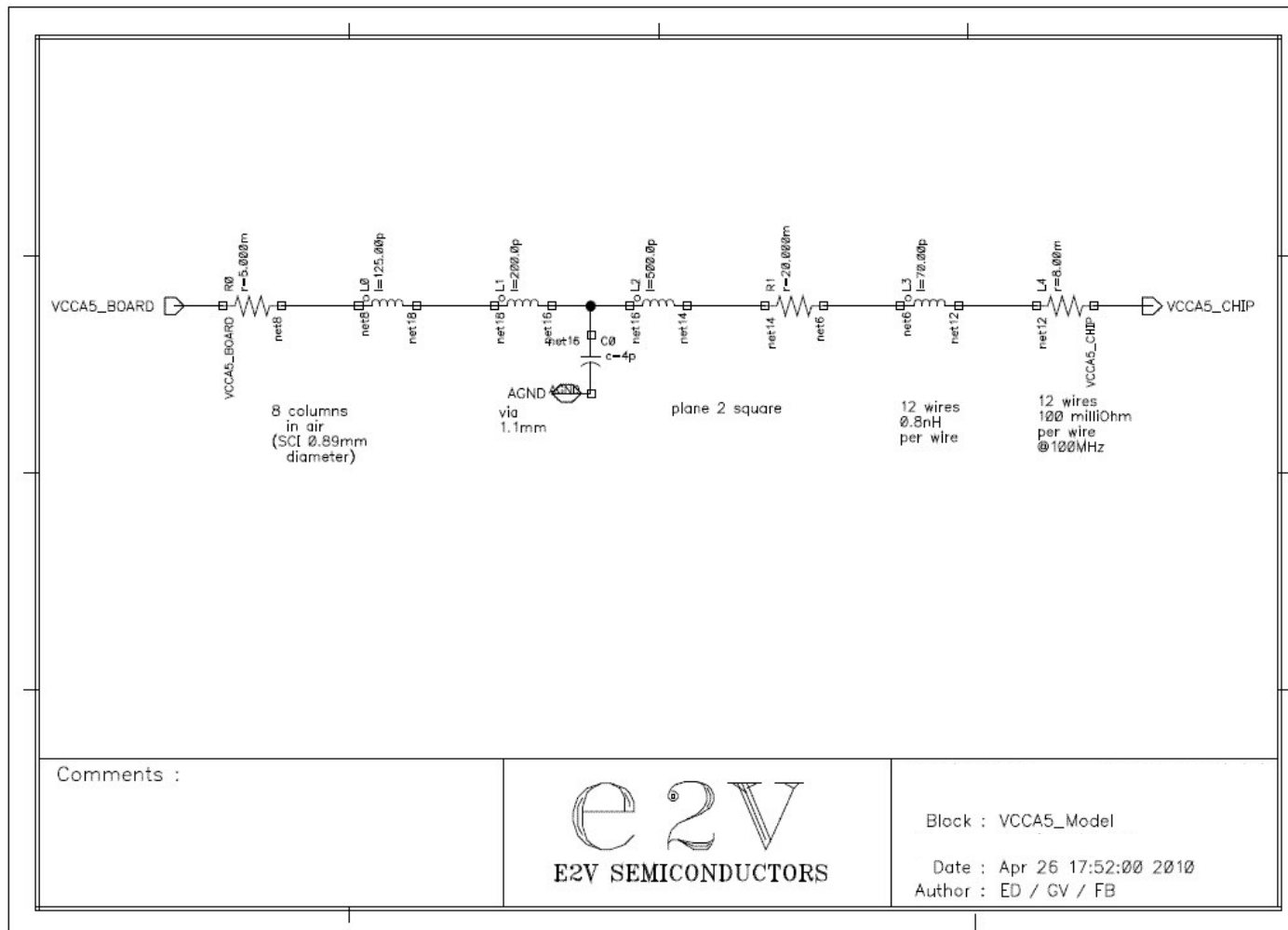
Ground Package Model AGND & DGND

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Power Supply Package Model VCCA5

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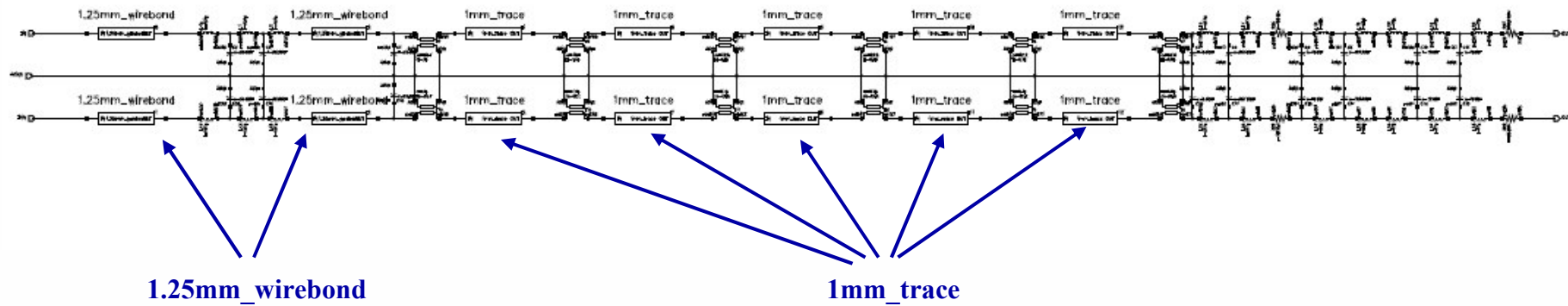


Analog Output Lines Package Models

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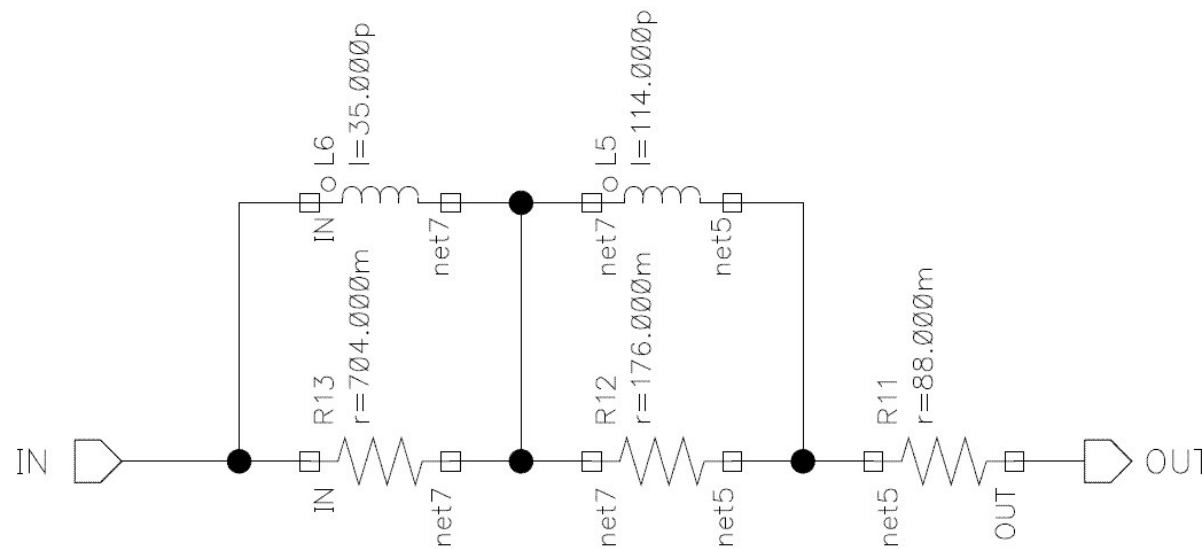
From Analog_Output_Model

To External Generators



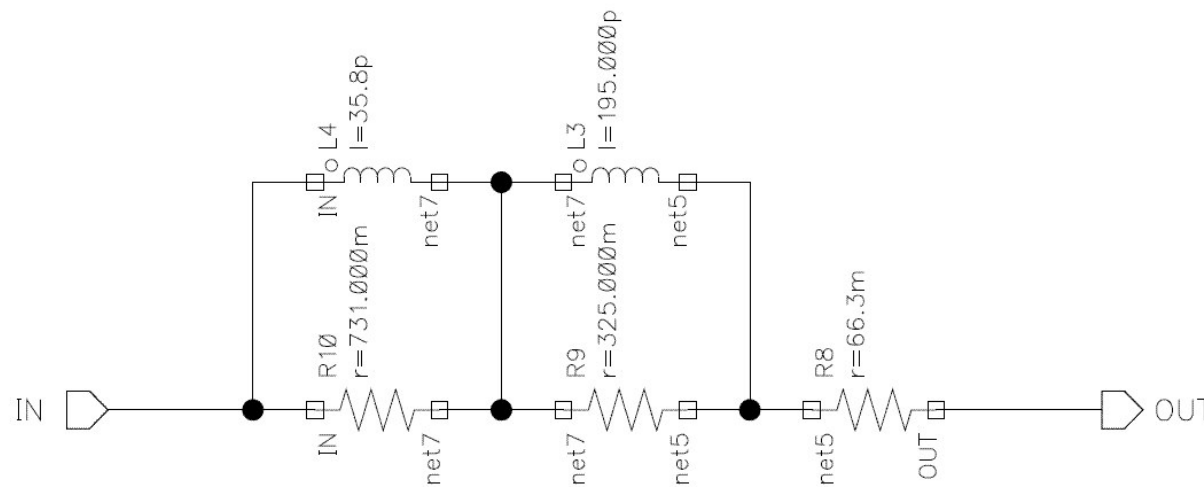
I/O Lines Package Model 1mm trace

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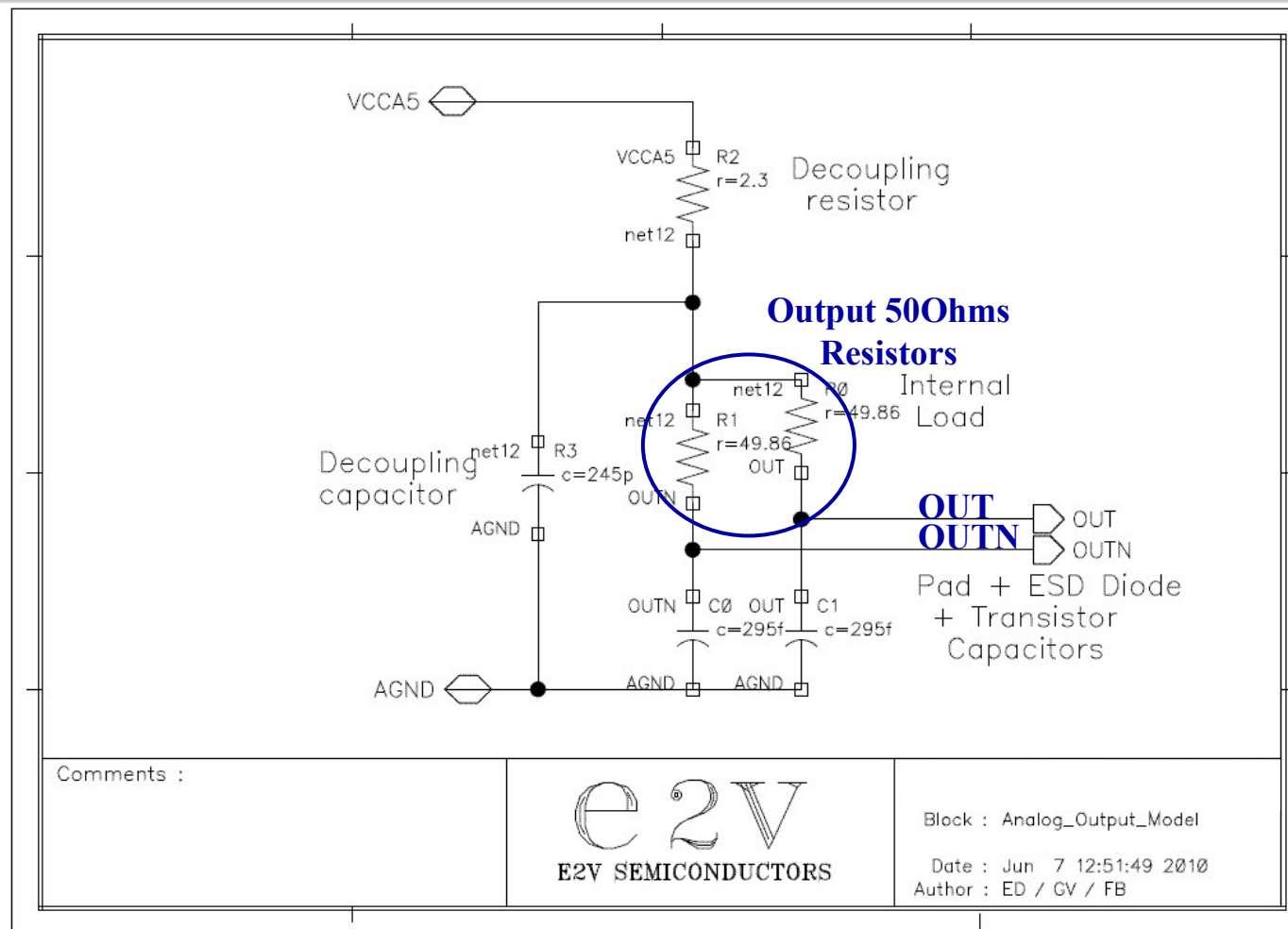
I/O Lines Package Model 1.25mm wirebond

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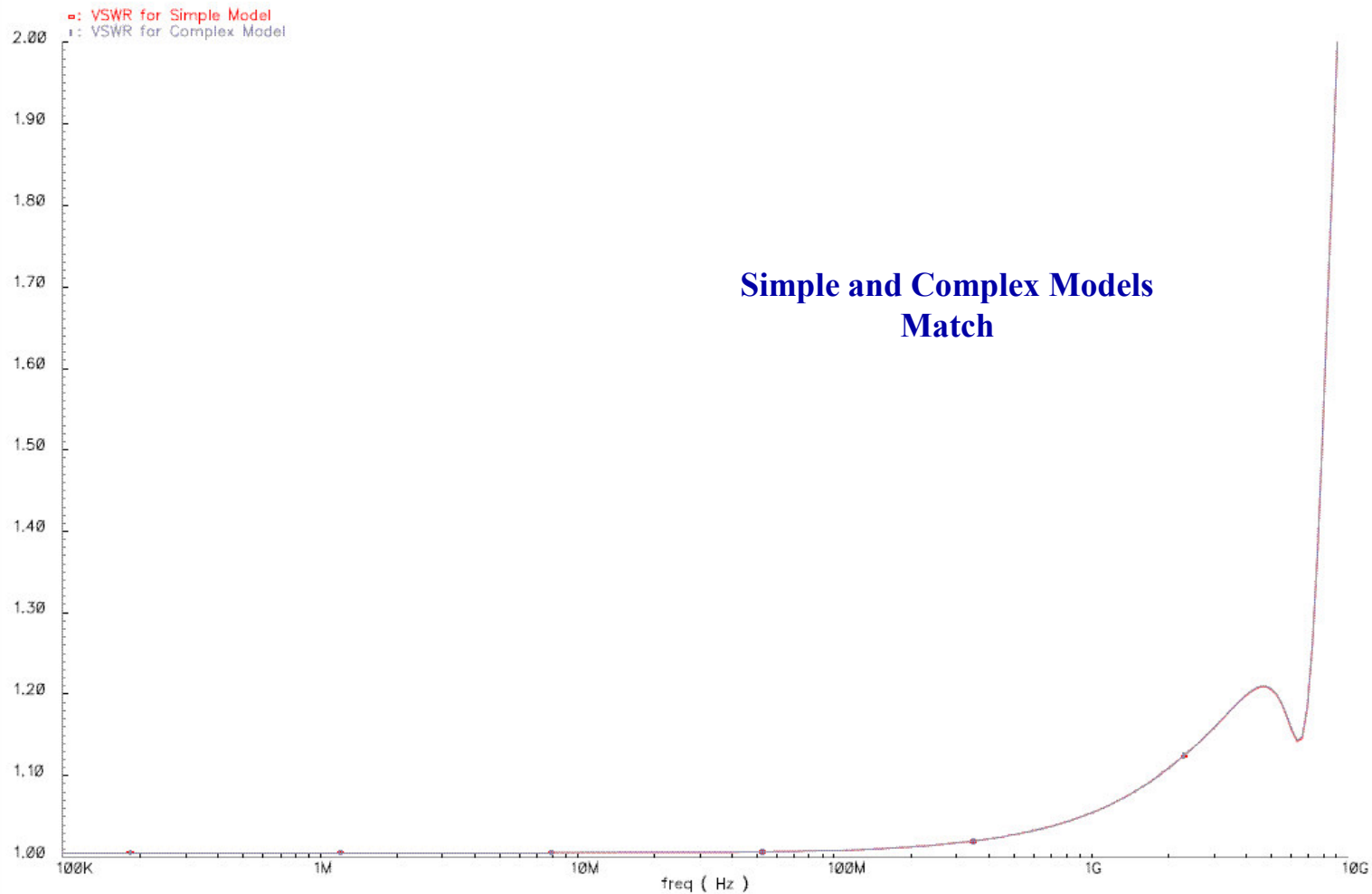
Analog Output Buffer Schematic (simplified model)

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Analog Output VSWR Response (Spectre) @27 °C; from 100Hz to 10GHz

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Analog Output VSWR Response (Spice) @27°C; from 100Hz to 10GHz

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